ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

A REVIEW OF 2.4 GHZ LNA USING DIFFERENT TOPOLOGIES IN STANDARD CMOS

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DOI: 10.5281/zenodo.49705

ABSTRACT

This paper presents the literature review of various designs of LNA using different topologies. Designing very high-performance LNAs is an active research area and is of crucial importance for wireless technologies. CMOS LNA architectures can be divided into two major groups the common source and the common gate LNA. CS LNA output gate current noise increases with the increase in frequency. In CGLNA noise factor is nearly constant irrespective of the frequency of operation and bandwidth.

KEYWORDS:

INTRODUCTION

The performance of any wireless communication system is limited by (RF) front-end. In wireless technology higher data rates, low-cost and compact designs are in demand due to large data transfer and market competition. These demands push stringent constraints on wireless and its supporting technologies that comprise the front-end. These challenging circuits prove to be a limiting factor in restricting bandwidth, range and sensitivity of RF communication systems. The typical block diagram for a heterodyne receiver is shown in Figure 1.1. Low-Noise Amplifier, Mixer, Variable Gain Amplifier and Voltage-Controlled Oscillator are the basic components of a heterodyne receiver. LNA is usually preceded by a band-pass filter which filters the out of band signals while allowing the in-band signals to pass through. After LNA there is a Mixer that is used for frequency translation of signals. Voltage Controlled Oscillator is used for frequency generation. IF filter is used to pass fixed Intermediate Frequency and signal moves to back end for digital processing.

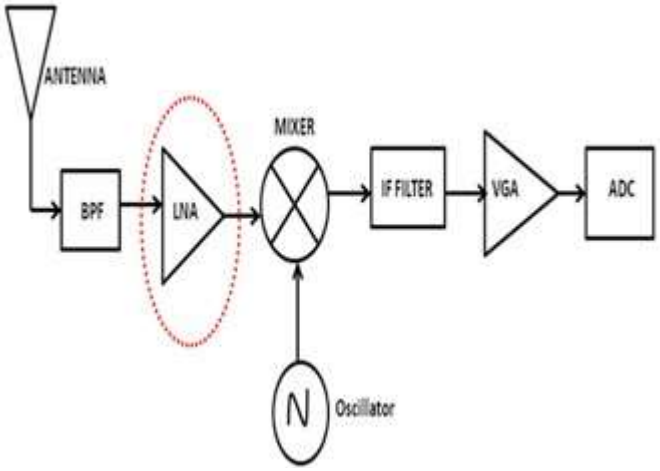

Figure 1: Typical Heterodyne Receiver Front-end

There is a growing demand of RFIC design to make device size small, portable and large frequency band applications. There are challenges like power consumption, high gain, low noise figure, high linearity. As the ISM band is a free platform. A number of designs of LNA are presented in literature by using different topologies and

techniques for ISM Band. This paper presents brief review of the research done by various researchers in the area of designing of LNA by simple current reuse, cascade amplifiers, cascoded amplifiers topology, source degeneration topology, resistive feedback, cross coupled capacitor technique, g_m-boosted current reuse topology, single stage, multistage designs which are the best design techniques.

One of the most efficient techniques is inductive degeneration because during its analysis it provides resistive component in the absence of resistor. It reduces power dissipation and thermal noise. Based on the input matching and noise performance, CMOS LNA architectures can be divided into two major groups the common source and the common gate LNA.

STUDY OF EXISTING TECHNIQUES

Without studying earlier work done by researchers/scientists we can't update our knowledge in respective field. The earlier techniques and concepts given by researchers are very helpful for analysing the present high technology communication era. There is a growing demand of RFIC design to make device size small, portable and large frequency band applications. This paper presents brief review of the research done by various researchers in the area of designing of LNA by simple current reuse, cascade amplifiers, cascoded amplifiers topology, source degeneration topology, resistive feedback, cross coupled capacitor technique, g_m-boosted current reuse topology, single stage, multistage designs which are the best design techniques. It is very essential to keep high gain with linearity and a low noise figure. The following literature review discusses all the above techniques.

W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. Pineda de Gyvez, D. J. Allstot, and E. Sanchez-Sinencio (2005) proposed a capacitor cross-coupled g_m-boosting technique to reduce the power consumption and improve the NF of a CGLNA. Conventional CGLNA exhibits a relatively high NF at low operating frequencies, which has limited its adoption notwithstanding its superior linearity, input matching and stability compared to the inductively degenerated CSLNA. This technique retains the advantages of the CGLNA topology. The technique also enables a significant reduction in current consumption. The fully integrated differential LNA consumes 3.6 mA from 1.8 V and attains a measured NF of 3.0 dB at 6.0 GHz. The proposed technique makes the CG topology attractive for low-power and high-frequency fully integrated designs.[1]

Taeksang Song, Hyoung-Seok Oh, Songcheol Hong, Euisik Yoon, (2006) proposed a 2.4-GHz fully integrated CMOS receiver front-end using current-reused folded-cascode circuit in a 0.18 μm technology. Vertically stacked LNA and a folded-cascode mixer was proposed to improve both conversion gain and noise figure suitable for sub-mW receiver circuits. Front-end achieves a conversion gain of 31.5 dB and a noise figure of 11.8 dB at 10 MHz with 500 μA bias current from a 1.0 V power supply. The conversion gain and noise figure improvements of the proposed front-end over a conventional merged LNA and single-balanced mixer are 11 dB and 7.2 dB at 10 MHz, respectively, with the same power consumption of 500 μW.[2]

Stanley B. T. Wang, Ali M. Niknejad, Robert W. Brodersen (2006) proposed a sub-mW UWB fully differential CMOS LNA operating below 960 MHz for sensor network applications. They utilized both NMOS and PMOS transistors to boost the transconductance, coupling the input signals to the back-gates of the transistors and combining the common-gate and shunt-feedback topologies. The LNA achieves 13 dB of power gain, a 3.6 dB minimum noise figure and -10 dBm of IIP3 with only 0.72 mW of power consumption from a 1.2 V supply.[3]

Yi-Jing Lin, Shawn S. H. Hsu, Jun-De Jin,C. Y. Chan (2007) presented a 3.1–10.6 GHz UWB LNA that utilized a current-reused technique. A different wideband technique with a simple high-pass filter as the input matching network was proposed. To reduce the signal loss and undesired noise coupling the GCPW structures was used in the layout. The implemented LNA presents a maximum power gain of 16 dB and a good input matching of 50 Ω in the required band. An excellent NF of 3.1–6 dB was obtained in the frequency range of 3.1–10.6 GHz with a power dissipation of 11.9 mW under a 1.8 V power supply using .18 μm CMOS technology.[4]

Yuna Shim, Chang-Wan Kim, Jeongseon Lee, and Sang-Gug Lee (2007) proposed a two-stage, common-gate in cascade with cascode topology. An optimized common-gate in cascade with cascode UWB LNA shows UWB input matching and nearly flat noise figure for 3.1 to 10.5 GHz band application. The noise figure of the proposed

common-gate topology reduces to F≈1+γ/2 and this is the advantageous noise figure characteristic of the common-gate topology which is not feasible with cascode or common-source topology. Commonly UWB LNAs adopt band-pass filters at the input, which lead to more than two inductors. Considering the limited quality factor of the inductors, especially the on-chip, but the proposed LNA can provide additional NF advantage as it adopts only one inductor at the input. The LNA was implemented in 0.18 m CMOS technology. This LNA has -10 dB input return loss, maximum gain of 16 dB and NF of 3.8- 4.0 dB over the full frequency band. It is dissipating 5.3 mA current from 1.8 V supply.[5]

Mikaël Cimino, Hervé Lapuyade, Yann Deval, Thierry Taris, and Jean-Baptiste Bégueret, (2008) proposed a self-testable and highly reliable low noise amplifier design in 0.13 µm CMOS technology for wireless local area networks to ensure data transmission. Proposed LNA was based on a built-in self test methodology. The test circuit was composed of one supply current sensor and one biasing voltage sensor, and it offers high fault coverage.[6]

Hsieh-Hung Hsieh, Jih-Hsin Wang, and Liang-Hung Lu, (2008) presented gain-enhancement techniques suitable for folded cascode LNAs at low-voltage operations using 0.18µm CMOS technology. A forward bias and a capacitive divider at the body of the MOSFETs were implemented. Due to suppression of the negative impact of the body transconductance, an enhanced gain was also maintained. In addition, g_m-boosting stage was introduced to further increase the LNA gain at the cost of circuit linearity. Measured dc power was 1.08mW from a 0.6-V supply voltage. The LNA with the forward-body-bias technique demonstrates a gain of 10.0 dB, noise figure of 3.37 dB and for the LNA with a G_(m)boosting feedback, a remarkable gain of 14.1 dB was achieved with a dc power of 1.68 mW. The measured P_in1dB is -18 dBm and〖 IIP〗_3 is -8.6 dBm.[7]

Baimei LIU1, Chunhua WANG1, Minglin MA, Shengqiang GUO (2009) proposed a low voltage and low power LNA with current-reused two-stage common source topology and modified input matching for minimizing the noise figure of the RF front end circuit. In case of CSLNA noise figure is higher as it is linear with the operating frequency so for minimizing noise figure a modified input matching circuit was used. By employing a modified current-reused architecture, the LNA can operate at a very low supply voltage with microwatt power consumption while maintaining reasonable circuit performance at 2.4 GHz. Using a TSMC 0.18 µm CMOS process, the fully integrated LNA exhibits a gain of 14.4 dB and a noise figure of 1.6 dB at 2.4 GHz, operated at a supply voltage of 0.9 V. The input matching (S_11) is –18.1 dB while consumes only 960 µW.[8]

Sanghoon Joo, Tae-Young Choi, Byunghoo Jung, (2009) proposed a new low-power LNA scheme which combines the merits of g_m-boosting from inductively degenerated topology and input impedance matching from resistive feedback topology. LNA schematic presented a g_m-boosted resistive feedback 2.4 GHz LNA using a series inductor matching network. The gain of the LNA increases by the Quality factor of the series resistor inductor caapacitor input network and its NF was reduced by a similar factor. By exploiting the g_(m) boosting property, the proposed fully integrated LNA achieved a noise figure of 2.0 dB, S_21 of 24 dB and IIP3 of -11 dBm while consuming 2.6 mW from a 1.2 V supply. [9]

Sambit Datta, Ashudeb Dutta, Tarnn Kanti Bhattacharyya (2010) proposed the design of fully concurrent dualband LNA architecture with concurrent input and output matching networks for application in the GSM & Bluetooth communication standards. An inter-stage inductor between the common source stage and the common gate stage was used to increase power gain. The architecture is called 'fully concurrent' because it uses the concurrent matching theory for both the input and output matching network. The dual-band LNA utilizes a common source single ended topology, which has distinct advantage compared to differential mode. Voltage gain of above 14 dB has been achieved in the frequency bands of interest with 2 dB noise figure. More selective load filter using active inductors and varactors were also proposed to minimize power consumption and design tunable multi-band LNAs.[10]

Meng Zhang, Zhiqun Li (2011) presented a low power low noise differential amplifier for wireless sensor network in TSMC 0.18 m RF CMOS process. A two-stage cascade CG topology and two external inductor choke coils were used to achieve input matching of LNA under low power consumption and a differential inductor has been designed as the load to achieve reasonable gain and reduce chip area simultaneously.[11]

Muhammad Khurram and S. M. Rezaul Hasan, (2012) proposed a design that takes the advantage of the current-reuse technique by "stacking" the active PMOS stage (that provides the inverting g_m-boosting gain between the source and the gate terminals of the input CG stage) on top of the input CG stage ("piggyback g_m-boosting"). The new proposed design reduced the power dissipation associated with the g_m-boosting, by implementing the "current-reused g_m-boosting", where the bias current is shared between the g_m-boosting CS stage and the amplifier CG stage. They represented a low-power CG UWB LNA architecture which implements a novel "current-reused-boosting" technique. The topology also includes a front-end passive LC-band-pass filter for broadband input matching with sharp out-of-band roll-off. Proposed architecture represents a low-power CMOS transconductance "g_m" boosted CG UWB LNA, operating in the 3–5 GHz range, employing current-reuse technique.[27]

Deyun Cai, Yang Shang, HaoYu, and Junyan Ren (2013) proposed an ultra-low-power design of two 60-GHz direct-conversion receivers in a 65-nm CMOS process for single-channel and multi-channel applications under the IEEE 802.15.3c standard, respectively. The given architecture has high gain 55 dB for single channel and 62 dB for multi-channel. One three-stage low-noise amplifier employs high- passive matching. A double-layer-stacked inductor is utilized for matching in the single-channel receiver and a high-impedance transmission line is utilized for matching in the multi-channel receiver, respectively. A modified Cherry–Hooper amplifier is applied for the variable-gain amplifier, to achieve high gain-bandwidth product and high power efficiency. The single-channel receiver is implemented with 0.34-mm chip area. power consumption is 8 mW, a minimum single-sideband noise figure (NF) of 4.9 dB, a 3-dB bandwidth of 3.5 GHz, and a maximum conversion gain of 55 dB. The multi-channel receiver is implemented with 0.56-mm chip area. It is measured with a power consumption of 12.4 mW, a 3-dB bandwidth of 8 GHz (59.5 67.5 GHz), and a maximum conversion gain of 62 dB. The measurement results show that the two demonstrated 60-GHz direct-conversion receivers can achieve high gain and low NF with ultra-low power in 65-nm CMOS.[13]

Boyu Hu, Xiao Peng Yu, Wei Meng Lim, and Kiat Seng Yeo, (2014) proposed a CMOS low-noise amplifier (LNA) for ultra wideband universal radio architecture. Based on capacitive cross coupled dual-g_m-enhancement topology, the circuit topology could be reconfigured as different versions for single-ended or differential inputs. Both a differential-input-differential output and a single-ended-input-differential-output version are fabricated in 0.18 μm CMOS technology. The differential input version achieves an 11–14 dB S_21, ≤ −9 dB S_11 within 1.4– 11.4 GHz, and a minimum noise figure of 3.9 dB; the single ended-input version achieves a 5–8 dB S_21,≤ −10 dB S_11 among 2.4–11.7 GHz, and a minimum noise figure of 6.3 dB.[14]

Ping-Yi Wang, Yun-Chun Shen, et al.(2015)
proposed the design and analysis of a high performance receiver front-end for various X-band applications. The proposed circuits employ transformer feedback and resonant-coupled networks (RCNs) for the low-noise amplifier (LNA). The mixer design uses a double-balanced topology to achieve low power and also low noise characteristics. The IF post-amplifier adopts the Cherry-Hooper based variable gain amplifier (VGA) with 3D inductors for wideband and high linearity considerations. Design is implemented in a 90-nm CMOS process with a dissipation of only 22.8 mA from a 1.2-V supply voltage. The measured NF is below 3.8 dB with a maximum conversion gain of 65.1 dB within the X-band of 8 -12 GHz. The average output P1dB over this frequency range is measured as 1.12 dBm at the maximum gain.[15]

The main objective of this paper is to develop a 1.4V 2.4 GHz LNA with minimum power dissipation using CMOS process. TSMC 0.18 μm CMOS technology has been chosen for the design. ADS software which provides a user friendly environment is used for the simulation of proposed LNA. The target specifications of the LNA are listed in table 1.1

Table 1.1 Target specifications of the LNA

Categories	Specifications
Noise figure	≤ 2 dB
S_{11}	≤ -10 dB
S_{22}	≤ -10 dB
IIP3	≤ -10 dBm
S_{21}	≥ 15 dB
S_{12}	≥ -20 dB
Stability factor	> 1
Input Impedance	50 Ω
Output Impedance	50 Ω

CONCLUSION

In the published literature, several techniques have been reported to impart high performance LNA design. In four techniques resistive termination, series shunt feedback, common gate connection and inductive degeneration that are used for matching, the most efficient technique is inductive degeneration because during its analysis it provides resistive component in the absence of resistor. It reduces power dissipation and thermal noise. The noise factor of the CG LNA depends on the device size and process parameters. The noise factor of the CS LNA with inductive source degeneration is linear with the operating angular frequency and it can be large in the GHz range. Future aspect these two topologies Common Source and Common Gate can be compared with respect to their noise figure.

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